REMARKS/ARGUMENTS

Claims 1-13 are pending in this application. By this Amendment, Applicant AMENDS claims 1-13.

The drawings were objected to for failing to show the "current controlling transistor." Applicant respectfully submits that the current controlling transistor is depicted in the drawings as element number 10, see, for example, element 10 in Fig. 3 of Applicant's drawings. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objection to the drawings.

The specification was objected to for allegedly failing to provide information about the variable "N." Applicant respectfully submits that, as is discussed in, for example, the paragraph bridging pages 15 and 16 of the Applicant's specification, N is a variable related to the size of the first transistor 11 and the current detection transistor. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this objection to the specification.

The specification was also objected to for allegedly failing to provide information about the "current controlling transistor." Applicant respectfully submits that the current controlling transistor is clearly described in the specification in, for example, the paragraph bridging pages 20 and 21 of the Applicant's specification. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this objection to the specification.

Claim 9 was objected to for allegedly containing minor informalities. Applicant has amended claim 9 to correct the minor informalities noted by the Examiner. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objection to claim 9.

Claims 1-13 were rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite. Applicant respectfully submits that the proportional current and the current controlling transistor that are recited in claims 1, 2, 8, and 9 are clearly described, for example, in the paragraph bridging pages 15 and 16, and the paragraph bridging pages 20 and 21 of the Applicant's specification. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1-13 under 35 U.S.C. § 112, second paragraph.

Claims 1-7 were rejected under 35 U.S.C. § 102(b) as being anticipated by Yamamoto et al. (U.S. 6,424,131). Claims 8-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamamoto et al.

Applicant respectfully traverses the rejections of claims 1-13.

Claim 1 has been amended to recite:

> A current detection circuit comprising:
> a first transistor arranged to supply load current to a load;
> a current detection transistor having a control electrode arranged to receive the same control signal as applied to the control electrode of said first transistor, said current detection transistor arranged to supply a proportional current that is proportional to said load current;
> **a buffer circuit having an idling current source arranged to supply a predetermined idling current to an output node of said current detection transistor, said buffer circuit arranged to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and arranged to output a detection current that amounts to the sum of said proportional current and said idling current; and**
> **a conversion circuit arranged to convert said detection current outputted from said buffer circuit into an output signal**. (emphasis added)

Applicant's claim 2 recites features that are similar to the features recited in Applicant's claim 1, including the above-emphasized features.

With the unique combination and arrangement of features recited in Applicant's claim 1, including the features of "a buffer circuit having an idling current source arranged to supply a predetermined idling current to an output node of said current detection transistor, said buffer circuit arranged to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and arranged to output a detection current that amounts to the sum of said proportional current and said idling current" and "a conversion circuit arranged to convert said detection current outputted from said buffer circuit into an output signal," Applicant has been able to provide a circuit that enables detection of a load current with reduced power consumption when compared to conventional circuits (see, for example, the paragraph bridging pages 9 and 10 of Applicant's specification).

The Examiner alleged that Yamamoto et al. teaches all of the features recited in Applicant's claim 1, including "a buffer circuit having an idling current source **(current source 12 provides current to node Q)** for supplying a predetermined idling current to an output node of said current detection transistor **(2)**, said buffer circuit adapted to equalize the output voltage of said first transistor **(1)** with the voltage at said output node of said current detection transistor **(2)**, and adapted to output a detection current that amounts to the sum of said proportional current and said idling current; and a conversion circuit **(6)** for converting into an output signal said detection current outputted from said buffer circuit **(col. 16, line 50 - col. 39, line 62)**." (emphasis in original)

Applicant respectfully disagrees for the following reason.

Claim 1 recites the features of "a buffer circuit having an idling current source arranged to supply a predetermined idling current to an output node of said current detection transistor, said buffer circuit arranged to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and arranged to output a detection current that amounts to the sum of said proportional current and said idling current" and "a conversion circuit arranged to convert said detection current outputted from said buffer circuit into an output signal."

Yamamoto et al. teaches a circuit including an output transistor 1, auxiliary transistor 2, current source 12, and current detecting resistance 6, as shown in Figs. 1 and 5A of Yamamoto et al. However, contrary to the Examiner's allegations Yamamoto et al. does not teach a circuit that includes *both* the current source 12 and the current detecting resistance 6. For example, column 19, lines 12-18 and column 21, lines 29-40 of Yamamoto et al. (which describe the separate embodiments shown in Figs. 1 and 5A of Yamamoto et al.) teach that the circuit of Yamamoto et al. *includes **either** the current source 12 **or** the current detecting resistor 6*. Thus, Yamamoto et al. *does not teach a circuit including **both** a buffer circuit and a conversion circuit* as is recited in Applicant's claims 1 and 2.

Thus, Yamamoto et al. clearly fails to teach or suggest the features of "a buffer circuit

having an idling current source arranged to supply a predetermined idling current to an output node of said current detection transistor, said buffer circuit arranged to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and arranged to output a detection current that amounts to the sum of said proportional current and said idling current" and "a conversion circuit arranged to convert said detection current outputted from said buffer circuit into an output signal" as recited in Applicant's claim 1 and similarly recited in Applicant's claim 2.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 1 and 2 under 35 U.S.C. § 102(b) as being anticipated by Yamamoto et al.

Claim 8 has been amended to recite:

> A load drive circuit arranged to perform pulse-width-modulated driving of a single-/multi-phase load, said load drive circuit having at least two series circuits such that each of said series circuits includes: a first transistor coupled between a first power supply voltage and the output node connected to said load to supply load current to said load when switched on by a switching signal; and a second transistor coupled between a second power supply voltage and said output node and switched on and off by a pulse-width-modulated switching signal, and that said series circuits together define a single-/multi-phase bridge circuit arranged to drive said single-/multi-phase load, wherein:
>
> each of said series circuits comprises:
>
> a current detection transistor arranged to receive the same switching signal as the switching signal supplied to said first transistor to provide a proportional current proportional to said load current; and
>
> **a buffer circuit having an idling current source arranged to provide a predetermined idling current to the output node of said current detection transistor, said buffer circuit arranged to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and arranged to output a detection current that amounts to the sum of said proportional current and said idling current**; and
>
> said load drive circuit further comprises **a conversion circuit arranged to collectively convert into an output signal the detection currents outputted from the respective buffer circuits**. (emphasis added)

Applicant's claim 9 recites features that are similar to the features recited in Applicant's

claim 8, including the above-emphasized features

The Examiner alleged that Yamamoto et al. teaches all of the features recited in Applicant's claim 8, including "a buffer circuit having an idling current source **(current source 12 provides current to node Q)** for providing a predetermined idling current to the output node of said current detection transistor **(2)**, said buffer circuit adapted to equalize the output voltage of said first transistor **(1)** with the voltage at said output node of said current detection transistor **(2)**, and adapted to output a detection current that amounts to the sum of said proportional current and said idling current, and characterized in that said load drive circuit further comprises a conversion circuit **(6)** for collectively converting into an output signal the detection currents outputted from the respective buffer circuits **(col. 16, line 50 - col. 39, line 62)**." (emphasis in original)

Applicant respectfully disagrees for the following reasons.

Claim 8 recites the features of "a buffer circuit having an idling current source arranged to provide a predetermined idling current to the output node of said current detection transistor, said buffer circuit arranged to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and arranged to output a detection current that amounts to the sum of said proportional current and said idling current" and "a conversion circuit arranged to collectively convert into an output signal the detection currents outputted from the respective buffer circuits."

First, as described above, Yamamoto et al. *does not teach a circuit including **both** a buffer circuit **and** a conversion circuit*. Furthermore, Yamamoto et al. does not include any suggestion or teaching that it would be desirable to include both a buffer circuit and a conversion circuit in the same system. Accordingly, one of ordinary skill in the art at the time of the invention would not have been motivated to add the buffer circuit of the first embodiment, shown in Fig. 1 of Yamamoto et al., with the conversion circuit of the second embodiment, shown in Fig. 5A of Yamamoto et al., because Yamamoto et al. teaches that these arrangements are used as replacements for one another, as described in column 23, lines 28-58 of Yamamoto

et al.

Furthermore, even assuming, *arguendo*, that one having ordinary skill in the art at the time of the invention would have been motivated to combine the separate embodiments shown in Figs. 1 and 5A of Yamamoto et al., the circuit resulting from this combination would still fail to teach each and every one of the features recited in claims 8 and 9. For example, nowhere in Yamamoto et al. is there any teaching or suggestion of the buffer circuit:

1) including an idling current source arranged to supply a predetermined idling current to an output node of the current detection transistor;

2) being arranged to equalize the output voltage of said first transistor with the voltage of the output node of the current detection transistor; or

3) being arranged to output a detection current that amounts to the sum of the proportional current and the idling current.

Thus, Yamamoto et al. clearly fails to teach or suggest the features of "a buffer circuit having an idling current source arranged to provide a predetermined idling current to the output node of said current detection transistor, said buffer circuit arranged to equalize the output voltage of said first transistor with the voltage at said output node of said current detection transistor, and arranged to output a detection current that amounts to the sum of said proportional current and said idling current" and "a conversion circuit arranged to collectively convert into an output signal the detection currents outputted from the respective buffer circuits," as recited in Applicant's claim 8 and similarly recited in Applicant's claim 9.

Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection of claims 8 and 9 under 35 U.S.C. § 103(a) as being unpatentable over by Yamamoto et al.

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1, 2, 8, and 9 are allowable. Claims 3-7 and 10-13 depend upon claims 1 and 8, and are

therefore allowable for at least the reasons that claims 1 and 8 are allowable.

In view of the foregoing amendments and remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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